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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,097	02/13/2004	Jae-jun Moon	Q77183	4555

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EXAMINER

ZWEIZIG, JEFFERY SHAWN

ART UNIT PAPER NUMBER

2816

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/777,097

Applicant(s)

MOON ET AL.

Examiner

Jeffrey S. Zweizig

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 3 remain rejected under 35 U.S.C. 102(b) as being anticipated by Wu et al. (USPN 5,307,007).

Fig. 1 discloses a bias circuit M1-M4 & R1, an output node (node between M1 & M3) and a start up capacitor C1 as recited in claim 1.

Fig. 3 discloses a bias circuit M3-M8/R1, an output node (node between M4 & M6, first MOS transistors M7 & M8, second MOS transistors M5 & M6 and start up capacitors C1 & C2 as recited in claim 3.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-4 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (USPN 5,180,967) in view of Wu et al..

Yamazaki Fig. 1 discloses a bias circuit 104/106/110/112/114 and an output node N11 or N12 as recited in claim 1. Further shown are start up circuits 118 & 120. Not shown is a start up capacitor as recited in claim 1. Wu et al. Figs. 1, 2, 4 & 6 disclose similar bias circuits including a start up capacitor C1 or C2. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the start up circuits 118 & 120 with a start up capacitor as taught by Wu et al. for the benefit of reducing component count and static current consumption. Claim 1 is obvious.

Yamazaki Fig. 1 further discloses a first PMOS 106, a second PMOS 104, a first NMOS 110, a second NMOS 112 and a resistor 114 as recited in claim 2. Claim 2 is obvious.

Yamazaki Fig. 5 discloses a bias circuit 104/106/124/126/130/128/114, an output node (node between 126 & 128, first MOS transistors 104 & 106 and second MOS transistors 124 & 126 as recited in claim 3. Further shown are start up circuits 118 & 120. Not shown are start up capacitors as recited in claim 3. Wu et al. Figs. 3 & 5 disclose similar bias circuits including a start up capacitors C1 & C2. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the start up circuits 118 & 120 with a start up capacitors as taught by Wu et al. for the benefit of reducing static current consumption. Claim 3 is obvious.

Yamazaki Fig. 5 further discloses a first PMOS 106, a second PMOS 104, a third PMOS 126, a fourth PMOS 124, a first NMOS 110, a second NMOS 112 and a resistor 114 as recited in claim 4. Claim 4 is obvious.

### ***Response to Arguments***

5. In reference to Applicants' arguments regarding the 102 rejection to claim 1, the output from the gate of M3 (Fig. 1) is an output of the circuit M1-M4, R1 and C. These are the components that are the subject of claim 1 and of the rejection. The output Vout is not part of the rejection and is irrelevant to the rejection. Furthermore, the arrangement of components M1-M4, R1 and C are the same as those claimed and would function the same. Likewise, the output from the gate of M4 (Fig. 3) is an output of the circuit M3-M8, R1, C1 and C2. These are the components that are the subject of claim 3 and of the rejection. The output Vout is not part of the rejection and is irrelevant to the rejection. Furthermore, the arrangement of components M3-M8, R1, C1 and C2 are the same as those claimed and would function the same.

In reference to Applicants' arguments regarding the 103 rejections to claims 1 and 3, as noted above, a node where an output is available is seen as an output. The references are seen to fully anticipate the output limitations of the claims. In reference to Applicants' arguments to claims 2 and 4, both references disclose circuits that are obviously symmetrical variations of one another. For example, Yamazaki Fig. 5 shows components 104, 102, 124, 126, 130 and 128, which are respectively analogous to Wu et al. Fig. 3 components M1, M2, M3, M4, M5 and M6, which are analogous to Applicants' Fig. 13 components MP91, MP92, MP93, MP94, MN95 and MN96.

### ***Conclusion***


6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey S. Zweizig whose telephone number is (571) 272-1758. The examiner can normally be reached on Monday thru Wednesday 6:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Jeffrey S. Zweizig  
Primary Examiner  
Art Unit 2816

JZ